FINAL PROGRESS REPORT
FOR
DEVICE ANNEALING STUDIES

CONTRACT NO. NAS 5-2755

1 April 1964 - 30 September 1964

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ELECTRIC CORPORATION



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Prepared By

AEROSPACE DIVISION

DEFENSE AND SPACE CENTER

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For

NASA GODDARD SPACE FLIGHT CENTER
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SUMMARY

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The objective of the present study is to develop an annealing process which can be used to achieve stable, high gain, bi-polar transistors for very low power applications.

This report is based on a series of experiments performed on wafers that were given several diffusions to form transistors. Electrical test showed that those transistors that were annealed at 700°C and 750°C in air for one hour had a lower gain and were leaky as compared with transistors that were pulled to the cool portion of the furnace and allowed to cool faster in the controlled atmosphere. Experiments performed with hydrogen annealing produced transistors with high gains. The mixing of various percentages of hydrogen and nitrogen permitted the amount of gain increase to be controlled. The hydrogen annealing system is described in deval as are the other annealing systems. Transistors were given a lead oxide deposition and annealed. The lead glass helps to stabilize the transistor characteristics and even increase the gains of previously untreated transistors.

It is now possible to achieve transistors with a range of gains. This can be done by using the correct mixture of hydrogen and nitrogen. A process is given based on the results of the experiments done on this contract.

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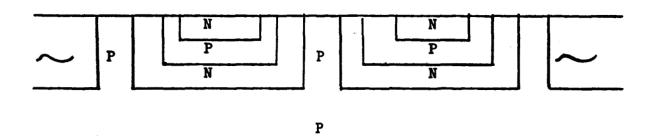


1.0 EXPERIMENTAL PROCEDURES

1.1 Device Structure

Two types of devices were initially selected for the annealing experiments. One was the transistor portion of an integrated amplifier block, and the other, a transistor design that was similar to the transistor of the amplifier.

A representative schematic of the transistor structure is shown below.



1.2 Sample Preparation

The silicon wafers used in the experiments were of 5 to 15 ohm cm, P type, doped with boron. The wafers were lapped with 12 micron Al_2O_3 grit from 17 mils to 13 mils. They were then lapped on one side to 11 mils using 3 micron Al_2O_3 grit and polished to 10 mils with 1 micron Al_2O_3 .

1.3 Device Fabrication

The wafers were cleaned after mechanical preparation to remove all traces of wax and grit by the following method:



The wafers were inserted in a holder so that each wafer was held separately. The holder was placed in a Soxhlet extractor so that clean trichloroethylene only was used to remove the wax. They were then heated in a 7% hydrogen peroxide solution to oxidize and remove the last traces of wax. The material was then placed on a boat and inserted into the epitaxial reactor. The wafers were etched in anhydrous HCl vapors for 40 minutes and then while in the same reactor a phosphorus doped n type epitaxial layer grown. The epitaxial layer was 20 microns thick and had a resistivity of 0.8 ohm cm. An oxide layer of 6000 A was grown on the wafers in the next step. The first mask was put on by photoengraving and holes etched in the oxide. The initial P type isolation diffusion separated the regions where the various transistors were to be diffused. The depth of the isolation diffusion was 25 microns to insure positive isolation. The resistivity of the diffusion was from 2 to 10 ohms per square. A 6000 A oxide layer was grown over the diffused layer. The second mask was put on by photoengraving and again holes were opened in the oxide for the P type base diffusion. The depth of the diffusion was 10 to 11 microns and had a resistivity of 250 to 300 ohms per square. A 6000 A oxide was grown over the diffused area. Photochemistry put on the third mask and opened holes in the oxide for the n type emitter diffusion of a resistivity of 2 ohms per square and a depth of 0.8 microns base width.

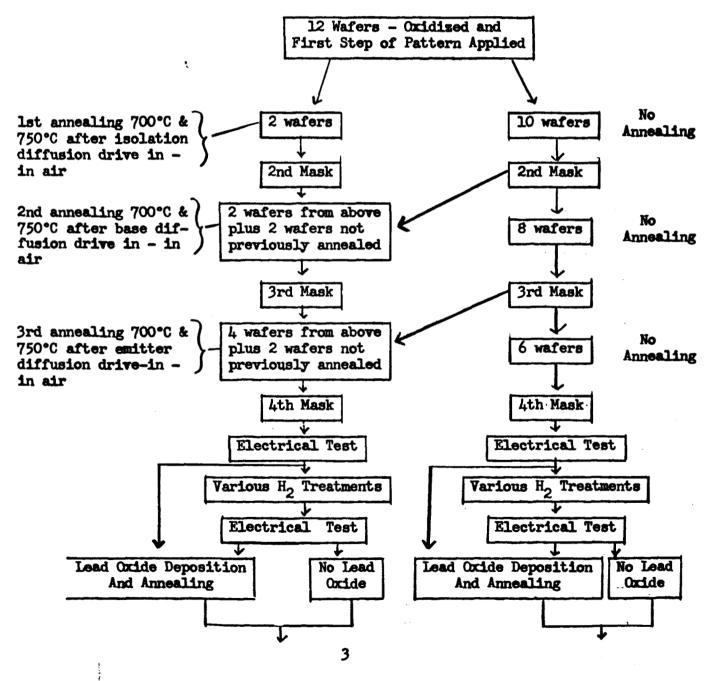
1.4 Annealing Procedure

The annealing temperatures of 700°C and 750°C were selected to minimize the formation of cristobalite in the oxide. The optimum temperature for the formation of cristobalite is at 800°C. The temperatures



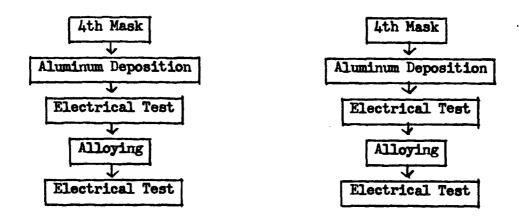
mentioned above were chosen with this in mind. If cristobalite has been formed then as cooling occurs and the temperature reaches 250°C X-("low")-cristobalite forms. This causes a drastic volume change and cracking occurs in the oxide. This would be detrimental for the subsequent diffusions.

The following is a block diagram of the procedure followed for the processing of the wafers:



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Twelve wafers were run in each of the first two experiments. Two wafers were annealed at 700°C after the boron isolation, these two plus two more were annealed after the boron base diffusion, these four plus two more were annealed after the phosphorus emitter diffusion. The annealing was done in the air atmosphere of the furnace hood.

The above was repeated for an annealing temperature of 750°C.

In a later experiment, the above procedure was followed but the annealing was done in the final atmosphere of the various diffusion runs. The final atmosphere of the isolation diffusion was 90% nitrogen and 10% oxygen while the base and emitter diffusions were done in an oxygen atmosphere.

The annealing was done in a small portable furnace with its own temperature controller. Each time the furnace was adjusted to the correct height.

In one series of experiments the wafers were given a hydrogen treatment for one-half hour at 800°C. The temperature was dropped by 50°C increments until 450°C. The boat was pulled out into the cool portion of the quartz tube and allowed to cool for about ten minutes. The



nitrogen was turned on and the hydrogen turned off. When the burn-off flame expired the boat was removed from the tube.

In another series of experiments nitrogen was mixed with the hydrogen in several varying proportions and for varying times. All experiments were performed at the same temperature of 800°C. One gaseous mixture consisted of H_2 -5 psig pressure, 500 cc/min., N_2 -10 psig pressure 1000 cc/min. Another mixture used was H_2 -5 lbs pressure, 500 cc/min., N_2 -10 lbs pressure 2000 cc/min. A third mixture was H_2 -5 lbs pressure, 1600 cc/min., N_2 -10 lbs pressure 1000 cc/min.

The lead oxide was evaporated on the wafers. In one series of tests only half of the wafers were coated with the lead oxide. Also, wafers that had not been hydrogen treated were coated with the lead oxide.

1.5 Apparatus

- The electrical power leads and the controller leads were made longer to facilitate the placing of the furnace into the various furnace hoods. Four adjustable legs were attached to the furnace. This was done to allow the boatload of wafers to go from the diffusion furnace directly into the annealing furnace without dropping below the annealing temperature. The quarts tube for the furnace was designed with a ground tapered end so that it could be inserted into the furnace tube. This permitted the wafers to be in the same atmosphere as the diffusion if desired.
- 1.5.2 The hydrogen annealing furnace was set up with safety in mind. The hydrogen and nitrogen lines were connected together with a tee



and then to the furnace tube. This permitted the tube to be flushed with nitrogen until all the air was flushed out. Then the hydrogen was turned on and the nitrogen turned off. The hydrogen was burned off at the exit end. The quartz tube was made long enough to accommodate the quartz boat out of the furnace and keep it in a hydrogen atmosphere until cooled to 100° C.

1.5.3 The third furnace was set up for the lead exide treatment. The first zone of the furnace was adjusted for $600^{\circ}\text{C} \pm 10^{\circ}\text{C}$. At this temperature the lead exide that was deposited on the wafers by vacuum deposition combined with the silicon diexide to form a lead-silica glass. The second some of the furnace was set at $400^{\circ}\text{C} \pm 10^{\circ}\text{C}$ to anneal the lead glass.



2.0 RESULTS

The wafers were tested on the 575A Tektronix Transistor tester for the gain and the $V_{\rm CEO}$ breakdown. The wafers that had been annealed in air were leaky and showed a lower gain and higher $V_{\rm CEO}$ breakdown voltage than the wafers that had not been annealed. The wafers that had been annealed in the same gaseous atmosphere as the diffusions did not show any significant difference in the gain or the $V_{\rm CEO}$ as the unannealed wafers.

Transistors on various wafers were electrically tested and the gains and $V_{\rm CEO}$ recorded. They were then given a hydrogen treatment for 15 minutes at 800°C. The transistors were electrically tested again. The gains were approximately tripled. Repeating the hydrogen treatment for another 15 minutes gave about the same readings. These same wafers were given a 30-minute treatment in a mixture of 2000 cc of N₂ and 500 cc of H₂ and tested. The gains decreased to approximately the same readings recorded when they were first tested. When these wafers were given a straight hydrogen treatment the gains went up. The gains resulting from this treatment were much higher than that recorded with the H2, N2 mixture. It was also found that in some cases repeated hydrogen treatments could cause channels. These channels in many cases could be removed by giving the wafer a 2 to 5 minute treatment in a furnace in an oxygen atmosphere. The temperature of the furnace was varied from 500°C to 800°C. A higher temperature can be used but for a shorter time. The oxygen treatment has the effect of reducing the gain while it removes the channel.



Electrical test of the wafers that had been partially coated with PbO and annealed in air showed that the coated area had improved gains as compared with the uncoated area. These gains, however, were not as high as those obtained by the hydrogen treatment. The lead glass stabilizes the transistor characteristics.

The wafers that had aluminum contacts vapor deposited and then alloyed and electrically tested showed a drop in the gain of the transistors.

Some of the transistors that were not metallized had been set aside for two months and retested. For that length of time the transistors had the same electrical characteristics as when first tested.



TABLE I

Comparison of the Gains of Annealed and Unannealed Transistors

Annealed

Unannealed

Transistor	β	A ^{CEO}	Transistor	β	ACEO
N-14-1	10	50	N-20-1	30	40
N-14-2	10	50	N-20-2	30	40
N-14-3	6	60	N-20-3	35	40
N-14-4	4	35	N-20-4	40	40
N-14-5	5	50	N-20-5	30	40
N-14-6	5	50	N-20-6	40	40

Annealing Done In Air At 700°C



TABLE II

Hydrogen Treatments

	As Di	ffused	Treatment I		Treat	Treatment II		Treatment III		ment IV	Treatment V
Transistor	β	A ^{CEO}	β	ACEO	β	A ^{CEO}	β	v _{ceo}	β	V _{CEO}	
U5 - 2	36	30	120	23	140	25	60	28	500	1.8	
V5 - 3	68	28	190	23	180	23	80	27	420	18	OTTA STORES
U5-4	68	28	130	25	140	25	50	32	440	18	CHANNELS
V5 - 5	110	25	280	20	280	20	160	24	400	19	DEVELOPED
U5 -1 6	50	28	340	20	340	20	140	26	580	17	
บ5-27	60	28	310	21	320	20	180	25	500	18	
บร-38	60	27	150	24	150	24	20	27	200	22	

psig Treatment I 1600 cc/min. 15 minutes at 800°C + 10°C H₂ 5 lbs pressure N₂ 10 lbs pressure 1000 cc/min. Treatment II H₂ 500 cc/min. 15 minutes at 800° C \pm 10° C 5 lbs pressure 2000 cc/min. N₂ 10 lbs pressure H₂ Treatment III 500 cc/min. 30 minutes at 800°C + 10°C 5 lbs pressure 2000 cc/min. 10 lbs pressure N₂ H₂ Treatment IV 5 lbs pressure 500 cc/min. 15 minutes at 800°C ± 10°C 1000 cc/min. N₂ 10 lbs pressure H₂ Treatment V 5 lbs pressure 1000 cc/min. 15 minutes at 800°C + 10°C 1000 cc/min. N₂ 10 lbs pressure



TABLE III

Hydrogen Treatments

	As Di	fused	sed Treatment I		Treatment II		Treatment III		Treatment IV		Treatment V	
Transistor	β	A ^{CEO}	β	A ^{CEO}	β	A ^{CEO}	β	v ceo	β	V _{CEO}	β	ACEO
N14-1	90	25	250	22	260	20	260	21	160	27	400	19
N14-2	70	28	150	25	240	22	180	23	50	29	350	20
N14-3	46	30	44	30	70	28	80	25	46	30	115	25
N14-4	60	27	150	25	150	24	100	25	50	28	210	22
N14-5	70	28	210	23	260	22	180	23	60	29	360	20
												e

psig

				P	2-2									
Treatment	I	H ₂	5	lbs	pressure	500	cc/min.	15	minutes	at	800°C	± 3	10°C	
		N ₂ 1	0.	lbs	pressure	1000	cc/min.							
Treatment	II	H ₂	5	lbs	pressure	500	cc/min.	15	minutes	at	800°C	±]	10°C	
		N ₂ 1	0.	lbs	pressure	1000	cc/min.							
Treatment	III	H ₂	5	lbs	pressure	500	cc/min.	15	minutes	at	800°C	<u> </u>	ro.c	
τ.		N ₂ 1	0.	lbs	pressure	2000	cc/min.							
Treatment	IA	H ₂	5	lbs	pressure	500	cc/min.	30	minutes	at	800°C	<u>±</u>]	ro•c	
		N ₂ 1	.0	lbs	pressure	2000	cc/min.							
Treatment	V	H ₂	5	lbs	pressure	1000	cc/min.	15	minutes	at	800°C	<u>+</u>]	10°C	



TABLE IV

Hydrogen, Lead Oxide, Alloying Treatment

	As Di	iffused	After H ₂ -80	0°C-½ hr.	After 02 Treatment, PbO and Alloying			
Transistor	β	ACEO	β	A ^{CEO}	β	A ^{CEO}		
N-12-1	8 c	30	400 c*	30	100	28		
N-12-2	6 c	20	400 c	25	100	30		
N-12-3	6 c	20	500 c	25	150	24		
N-12-4	8 c	20	500 e	30	150	24		
N-12-5	6 c	20	300 с	30	100	25		
N-12-6	6 c	20	500 c	28	325	24		

*c = Channels

TABLE V

Hydrogen, Alloying Treatment

	As Di	ffused	After H ₂	Treatment	After A	lloying
Transistor	β	ACEO	β	A ^{CEO}	β	A ^{CEO}
N-24-1	60	18	500	15	Leaky	10 No PbO Treatment
N-24-2	90	24	1000	20	Leaky	13 Sefore Alloying
N-24-3	80	25	800	20	150	Pb0 Treatment
N-24-4	60	20	1000	20	130	15 Before Alloying
N-24-5	120	20	1200	20	150	12) Belove Kiloying



TABLE IV

Effect of Lead Glass on Transistor Electrical Characteristics

Annealed Tra	Annealed Transistors			PbO Ann	nealed-Al	After	Alloying
1 T	β	A ^{CEO}	,β	V _{CEO}	β	V _{CEO}	
	N-14-1	10	50	200	25	150	25
All coated	N-14-2	10	51	150	25	150	25
with PbO	N-14-3	6	60	150	25	125	28
WICH PBO	N-14-4	4	35	175	25	150	28
	N-14-5	5	50	200	25	150	25
	N-14-6	5	50	175	25	125	25
	N-19-1	30	28	125	25	100	25
Coated	N-19-2	Leaky	0	100	28	75	28
with PbO	N-19-3	Leaky	0	125	28	100	28
	N-19-4	Leaky	0	100	28	75	28
Not coated	N-19-5	Leaky	0	70	28	10	30
with PbO	N-19-6	Leaky	0	50	28	50	28



3.0 DISCUSSION

3.1 Discussion and Results

The annealing of transistors in air at 700°C or 750°C for one hour was detrimental to the electrical characteristics - Table I. Annealing transistors in the same atmosphere that is used at the end of the diffusion did not result in any significant difference in the gain as those transistors that were not annealed. The use of a mixture of hydrogen and nitrogen increases the gain. The amount of gain can be "tailored in" by selecting the correct proportions of nitrogen and hydrogen. A particular transistor can be used in a number of different integrated circuits by adjusting the gain with the above gaseous treatment. The use of an extra furnace for the nitrogen, hydrogen treatment can be eliminated by the incorporation of this treatment in the final diffusion. That is, the regular diffusion is done but for the last two or three minutes the atmosphere is changed to the desired mixture by first flushing the furnace tube with nitrogen and then adjusting the nitrogen and adding hydrogen. If very high gains are needed then only hydrogen is used after flushing. Allowance should be made in calculating the amount of gain needed as it has been found (Table IV and VI) that metallization and alloying cause lowering of the gain. The use of lead oxide evaporation on the silicon dioxide layer before metallization is very desirable. It stabilized or "locks in" the transistor characteristics. In some cases it increased the gain without a hydrogen treatment.



3.2 Procedure

The following is then the recommended procedure for obtaining a stable, high gain bi-polar transistor for very low power application:

- 3.2.1 Prepare the wafer by slicing and planetary lapping with 12 micron Al_2O_3 grit until 2 mils of material are removed from both sides. Lap one side with 3 micron Al_2O_3 grit until 2 mils are removed. Polish the same side with 1 micron Al_2O_3 until 1 mil is removed. Remove the wafer from the polishing holder and clean off the wax. The final solvent rinse should be done in a Soxhlet extractor. Then immerse the wafers in a hot 7% hydrogen peroxide solution for twenty minutes and rinse thoroughly in deionized water.
- 3.2.2 Etch the surface of the wafer in a gaseous HCl etch or chemical polish to remove the mechanically damaged layer.
- 3.2.3 If the design includes an epitaxial layer, it is recommended that the epitaxial layer be deposited after the gaseous HCl etch so that it has a clean substrate.
- 3.2.4 Grow a 6000 Å oxide on the wafer and print the desired pattern by photoengraving.
- 3.2.5 Do the desired diffusions, using the process as developed under Contract No. NAS5-2755. After each diffusion the next pattern is applied by photoengraving.
- 3.2.6 At the last diffusion, either N type or P type, the run is terminated by purging the diffusion tube with nitrogen to remove the last



traces of moisture and/or oxygen. A mixture of 2500 cc/min. of H_2 and 500 cc/min. of N_2 is allowed to flow for ten minutes when the furnace is at 1000°C to obtain a high gain (See Table II for other conditions). At the end of the ten minutes, the boat is pulled to the cool portion of the furnace tube and allowed to cool in the same atmosphere.

Note: This procedure is followed when there is a good exhaust to remove the hydrogen. If this is not available it is recommended that a ground glass joint be attached to the furnace tube. Then a matching end-cap with an opening large enough to accommodate a quarts rod to pull the boat into the cool portion is attached. The hydrogen gas is burned at the exit of the end-cap.

- 3.2.7 Photoengrave and open holes in the oxide. Test.
- 3.2.8 Clean at 150°C in concentrated H₂SO₄ for 5 minutes, and rinse thoroughly to remove all traces of acid.
- Joad a platinum boat with a 50 milligram charge of high purity PbO (e.g. J. T. Baker Lead Oxide Cat. No. 2338). Evacuate the evaporator chamber to a minimum vacuum of 5 x 10⁻⁵ mm. The evaporation is done slowly. The platinum boat is used as a resistance heater and is heated carefully until the PbO becomes molten (approximately 890°C). Enough heat is maintained to keep the PbO molten. The evaporation is finished when all of the PbO has evaporated. The substrate is placed 9 inches above the source. The wafers are held on a portion in which there are no devices.

Note: The vacuum chamber should be used only for lead oxide evaporation.



3.2.10	Place in furnace in air atmosphere at 600°C for 30 m	inutes,
move into 400°C	ne and anneal for 30 minutes.	

- 3.2.11 Photoengreeve and open holes in oxide.
- 3.2.12 Evaporate metallic contacts.
- 3.2.13 Photoengrave and remove unwanted aluminum.
- 3.2.14 Alloy